Dr. KHALDOON MHAIDAT

Computer Engineering Department, JUST, P.O. Box 3030, Irbid 22110, Jordan

Phone: +962-772383737

E-mail: mhaidat@gmail.com; mhaidat@just.edu.jo

EDUCATION

Oregon Graduate Institute/OHSU, Portland, Oregon, USA

Ph.D. in electrical and computer engineering **2006**

Thesis: Representations and Circuits for Time Based Computation. Semiconductor Research Corporation (SRC) funded research project. Advisor: Prof. Marwan Jabri, Co-advisor: Prof. Dan Hammerstrom.

Oregon State University, Corvallis, Oregon, USA

M.S. in electrical and computer engineering **2002**

Thesis: Prototyping a Scalable Montgomery Multiplier using Field Programmable Gate Arrays (FPGAs). National Science Foundation (NSF) funded research project. Advisor: Prof. Alexandre Tenca, Co-advisor: Prof. Çetin Koç.

Jordan University of Science and Technology (JUST), Irbid, Jordan

B.S. in electrical and computer engineering **1999**

Full scholarship from Minstry of Higher Educaiton. Dean's honor list, Rank: 7 out of 102.

Jordan General Secondary Examination **1994**

Scientific stream, Score: 94.9%, Rank: 1st in Irbid 3rd district.

EXPERIENCE

Visiting Associate Professor – electrical engineering department, Prince Sumaya University for Technology (PSUT), Amman, Jordan	**9/2022 – Present**
Associate Professor – computer engineering department, JUST, Irbid, Jordan	**4/2015 – Present**
Faculty – electrical engineering, Higher Colleges of Technology (HCT), Dubai, UAE	**8/2016 - 7/2019**
Project Manager – industry collaboration with Silego Technology Inc., Santa Clara, Calfornia, USA.	**8/2012 - 1/2014**
Assistant Professor – computer engineering department, JUST, Irbid, Jordan	**9/2006 - 4/2015**
Chairman – computer engineering department, JUST, Irbid, Jordan	**9/2011 - 9/2012**
Adjunct Assistant Professor – New York Institute of Technology (NYIT), Amman, Jordan	**9/2010 - 6/2013**
Component Design Engineer – Desktop Platform Group, Intel Corporation, Santa Clara, California, USA	**3/2006 - 1/2007 (resigned)**
Graduate Technical Intern – Desktop Platform Group, Intel Corporation, Santa Clara, California, USA	**2/2005 - 9/2005**
Graduate Technical Intern – Microprocessor Design Group, Intel Corporation, Hillsboro, Oregon, USA	**6/2004 - 11/2004**
Graduate Technical Intern – Microprocessor Design Group, Intel Corporation, Hillsboro, Oregon, USA	**6/2003 - 1/2004**

Research Assistant – ECE, Oregon Graduate Institute/OHSU, Beaverton, Oregon, USA	**6/2002 - 3/2006**
Research Assistant – ECE, Oregon State University, Corvallis, Oregon, USA	**9/2000 - 6/2002**
Teaching Assistant – ECE, Oregon State University, Corvallis, Oregon, USA	**9/2001 - 12/2001**
Teaching Assistant – Computer Engineering, Yarmouk University, Jordan	**10/1999 - 7/2000**
Programmer – "Arabia.On.Line", Amman, Jordan	**7/1999 - 10/1999**
Intern – "Institut für Telematik", Trier, Germany	**7/1998 - 9/1998**

AWARDS

- Continuous Service Award from IEEE-TTTC, IEEE Computer Society.
- IBM faculty award ($7000) for the project entitled “Performance and power analysis of hypervisor based power management in many-core systems”.
- Best paper award for the paper: "FPGA-Based Features Extraction Unit for Arabic Characters," in the 4th International Conference on Information and Communication Systems, Irbid, Jordan, 2013.
- 3rd prize in the 5th international microelectronics Olympiad, Students’ Mentor.
- Intel Prescott (P4 90nm) achievements award
- Intel Cedarmill (P4 65nm) achievements award
- Intel kudos award for writing an automation script for speed-path debug which was critical to timely project completion in Cerdarmill P4 CPU
- Engineering Dean's honor list award.

SCHOLARSHIPS & FELLOWSHIPS

- Semiconductor Research Corporation (SRC) Ph.D. Fellowship.
- IAESTE-DAAD engineering internship awarded for top engineering students.
- Ministry of Higher Education scholarship for B.S. study.
- JUST scholarship for M.S. and Ph.D. study.

GRANTS & INDUSTRY FUNDED PROJECTS

- IBM faculty award ($7000) for the project entitled “Performance and power analysis of hypervisor based power management in many-core systems”. Project manager/Principal investigator.
- OpenSPARC Project fund and support from Sun Microsystems. SPARC T2 server (~$12000) + Four Virtex-5 FPGA development kits (~$6000) + membership and full access to SUN university program. Project manager/Principal investigator.
- Silego GreenPAK2 power supply design project fund ($8000) + Silego GreenPAK2 and GreepPAK3 programmable mixed-signal IC design evaluation kits + Cypress PSoC3 and PSoC5 development kits. Project manager/Principal investigator.
- Synopsys full North-America university full bundle (2-year 20-user license, $20M+ industry value) + membership and full access to Synopsys university program.
- Xilinx ISE full system edition (75-user license) + membership and full access to Xilinx university program.
- Mentor Graphics IDT’15 sponsorship fund ($6000).
- Jordan’s Competiveness Program (JCP) sponsorship of Jordan’s 1st MakerFair and Internet of Things Event, in parallel with IDT’15.

RESEARCH INTERESTS

- Image Recognition, OCR, Computer Vision, AI, ML, Robots.
- Embedded systems, Hardware Accelerators, FPGAs, ASICs, SoCs, CPUs, MCUs, GPUs.

- Power management and energy efficiency.
- Emerging IC devices, technologies, and sensors.
- Cryptography, intrusion detection (IDS).
- High performance computing (HPC), parallel computing.

PROFESSIONAL SERVICES & MEMBERSHIPS

- General chair of the IEEE IDT'15 Symposium, Dead Sea, Jordan.
- Chair of the organizing committee for ASET'18 multi-conferences, Dubai, UAE.
- Chairman of the CPE department at JUST during the academic year 2011/2012.
- Organizing committee member for ASET'19 multi-conferences, Dubai, UAE.
- TPC member for the IEEE International Design and Test Symposium (IDT)
- TPC member for the International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)
- TPC member for the International Conference on Information & Communication Systems (iCICS)
- TPC member for the IEEE Jordan Conference on Applied Electrical Engineering and Computing Technologies (AEECT)
- Editorial board member for the International Journal of Embedded and Real-Time Communication Systems (IJERTCS)
- Invited speaker at Khalifa University, Abu Dhabi, UAE. Seminar: "Algorithms and Scalable Architectures for Montgomery Modular Multiplication", April 13, 2016.
- Reviewer for the International Journal of Modeling and simulation
- Reviewer for the Journal of King Saud University - Computer and Information Sciences
- Reviewer for the International Journal of Electronics
- Committee member for the International Microelectronics Olympiad of Armenia organized and sponsored by Synopsys
- Active collaborator with Synopsys Armenia Educational Department (SAED) for EDA training, curriculum development, and research; received training myself and sending students for summer internships every year
- Liaison for Synopsys, Xilinx, and Sun/Oracle at JUST
- Founder and supervisor of the Circuits and Systems Research Lab and group at JUST
- Supervisor/co-supervisor of the thesis work of many MS students at JUST
- Thesis committee member for many MS students at JUST and other universities in Jordan including Yarmouk University, PSUT, and Jordan University.
- M.S. comprehensive exam committee member, CPE/JUST.
- Supervisor/co-supervisor of senior design projects of many BS students at both JUST and HCT/UAE.
- Member of the Graduate Studies Committee, CPE department and CIT College at JUST
- Member of the CIT College council, JUST
- Member of the Accreditation and Quality Assurance Committee, CPE department at JUST, ABET and MOH accredited.
- Chair/Member of the Curriculum Development Committee, CPE department at JUST
- Chair/Member of the Graduation Projects Committee, CPE department at JUST
- Member of the Scientific Research Committee, CPE department at JUST
- Chair/Member of the Course Schedule Committee, , CPE department at JUST
- Chair/Member of the Tenders and Labs Committee, CPE department at JUST
- Chair/Member of the Study Plans and Courses Transfer Committee, CPE department at JUST
- Member of the Scholarships and hiring Committee, CPE department at JUST
- Couse coordinator and course curriculum development committee for various courses at both JUST and HCT/UAE.
- Coordinated senior design projects and organized exhibitions and competitions at both JUST and

HCT/UAE.

- Judge for senior design projects competitions at both JUST and HCT/UAE.
- Academic Advisor for hundreds of students at JUST, PSUT, and HCT/UAE.
- Member of King Abdullah II School of Engineering Industry Committee, PSUT
- Member of Electronics Program Committee, EE department, PSUT
- Collaborated with Jordan Competiveness Program (JCP) to engage students in a nationwide competition – Jordan 1st MakerFair and Internet of Things Event, in parallel with IDT'15, Dead Sea Jordan.
- Panelist, "Electronics Design & Test Ecosystem in MENA Region", with Dr. Hazem ElTahawy GM of Mentor Graphics - Egypt and others, IDT'15, Dead Sea, Jordan.

PROFESSIONAL DEVELOPMENT TRAINING & WORKSHOPS

- Development of Curriculum & Study plans for Accreditation Board For Engineering And Technology (ABET)
- Modern University Instructional Methods
- Academic Testing and Evaluation
- PMP and CAPM certified training from PMI at HCT/UAE
- Multisim and LabVIEW training from NI at HCT/UAE
- Blackboard e-learning platform, HCT/UAE
- Moodle e-learning platform, JUST

TECHNICAL SKILLS

- C/C++, C#, JAVA, Perl, Python, Fortran , Shell scripting
- CGI, MySQL, POP3, socket programming, HTML
- Assembly programming: Intel, Motorola, ARM, MIPS, RISC
- MATLAB, Maple
- Parallel programming: OpenMP, MPI, CUDA
- UNIX, Linux, Windows, MS-DOS
- Verilog, VHDL, Verilog-A/MS, VHDL-A/MS, SPICE
- Intel: Opus, Presto, Lynx, iHDL, FRITS/KAVERI, MAX, ArchSim, Csim, TangoLR, Aspen, In-Target Probe (ITP) hardware & software, hands-on experience in Intel post-silicon debug labs
- Mentor Graphics: DesignArchitect, ModelSim, Eldo, AccuSimII, LeonardoSpectrum, ADMS, ICStation, Calibre
- Xilinx: Vivado HLS, ISE, iSIM, XMD, SDK, EDK, CoreGen, BSB
- Synopsys: VCS, Design compiler, IC compiler, Custom Designer, PrimeTime, HSPICE
- Cadence: OrCAD/PSpice, Virtuoso
- NI: Multisim, LabVIEW
- IMS Vanguard tester hardware & software
- PCB: ExpressPCB, EAGLE PCB, SMD soldering

EXAMPLE OF PROJECTS AND ASSIGNMENTS

- Representations & circuits for inter-pulse-interval (IPI) based computation & conversion: design, simulation, semi-custom layout, LVS & DRC verification, parasitics extraction, back-annotation, post-layout simulation, fabrication, & test of a TSMC 0.35um CMOS chip. Semiconductor Research Corporation (SRC) sponsored Ph.D. research.
- Speed path debug & micro-architecture validation for Cedarmill CPU: This includes using FRITS/KAVERI to generate pseudo-random long tests, loading & running tests on Merlin platform, extracting the data & instruction seeds for the worst case Orphan & generating the worst case trace to be run on the structural tester for speed path debug. It also includes writing IA-32/64 assembly & MAX tests that targets certain parts of the CPU for fault grading. It also includes using the NetBatch tools to

run & generate 20K+ golden traces per major Silicon stepping and debugging and fixing failures.

- Mixed signal validation for Cedarmill CPU: This includes using ADMS, Eldo, ModelSim, & Presto/Lynx for pre-silicon validation of mixed signal designs like the thermal sensor, rise & fall time control (RFTC), on-die VRM, DLLs, & PLLs.
- DFT design validation on Prescott CPU & analysis of performance parametrics from high volume manufacturing (HVM) test database: This includes using the IMS Vanguard tester & the ITP platform for post-silicon validation of DFT designs like I/O per-leg driver test (PLDT), I/O level generator (LevGen), on-die droop detector (ODDD), & DLLs.
- DC-DC buck converter circuit design using Silego's GreenPAK2 programmable mixed-signal array. Design was validated by designing and manufacturing a PCB using the ExpressPCB tool and service.
- Perl script that uses Intel unified data model (UDM) library to build the netlist of a Mega block in the Cedarmill CPU from ASPEN node reports which contain power vs. activity information. This tool was used to perform power optimization analysis.
- ITP program that automates platform-level programming & data collection of the ODDD circuit which helped in characterizing first, second, & third droops in Prescott.
- Design & simulation of an operational amplifier using TSMC 0.25um CMOS process, an operational amplifier, & a latching comparator (decision circuit & high sensitivity D flip-flop) using Maxim's GST2 bipolar process.
- ASIC implementation of a special peripheral-assisted microcontroller, which has a RISC core, a universal asynchronous receiver and transmitter (UART), a pulse width modulator (PWM), and a parallel input output port (PIO).
- ASIC-to-FPGA conversion of Montgomery multiplication based cryptographic processor.
- EPP2MM Interface circuit & driver which support EPP based communication between a PC and the Montgomery multiplication cryptographic processor residing on Digilent D2 FPGA board.
- Different FPGA implementations of the Montgomery multiplier for cryptography.
- RISC561 machine emulator, 2-pass assembler, and direct linking loader.
- Building and testing a Motorola 68000 based computer system.
- Porting MIPS R10000 super scalar processor to Stanford SimOS machine simulator.
- Virtual memory management system simulator.
- CGI/Perl web based status report submission & tracking tool.
- CGI/Perl scripts & specialized POP3 client that interface with a large hardware verification system.
- GITEX 2000 online database using Perl & mySQL under UNIX.
- Ethernet and Token-Ring networks simulation.
- Random access networks simulation: Pure Aloha, Slotted Aloha, CSMA, and CSMA/CD.

INVITED TALKS

- Seminar: "Algorithms and Scalable Architectures for Montgomery Modular Multiplication", Khalifa University, Abu Dhabi, UAE, April 13, 2016.
- Panel: "Electronics Design & Test Ecosystem in MENA Region", with Dr. Hazem ElTahawy GM of Mentor Graphics - Egypt and others, IDT'15, Dead Sea, Jordan.
- Presentation: "Proposal for IDT'15 in Jordan", to IDT steering committee, IDT'14, Algiers, Algeria.

RESEARCH PUBLICATIONS

1. E. Taqieddin, H. Al-Dahoud, K. Mhaidat, "Security Analysis and Improvement of Reconstruction Based Radio Frequency Identification Authentication Protocol", International Journal on Communications Antenna and Propagation, vol. 8, no. , pp. 221-206, 2018, Praise Worthy Prize.
2. M. Aldwairi, Y. Flaifel, K. Mhaidat, "Efficient Wu-Manber Pattern Matching Hardware for Intrusion and Malware Detection", 2018 International Conference on Electrical, Electronics, Computers.
3. Raed Bani-Hani, Khaldoon Mhaidat, Salah Harb, " Very Compact and Efficient 32-Bit AES Core Design

Using FPGAs for Small-Footprint Low-Power Embedded Applications," Journal of Circuits, Systems and Computers (JCSC), Volume 25, Issue 07, July 2016.
4. E. Taqieddin, O. Abu-Rjei, K. Mhaidat, "Efficient FPGA Implementation of the RC4 Stream Cipher using Block RAM and Pipelining," Procedia Computer Science, vol. 63, no. , pp. 8-15, 2015, Elsevier.
5. K. Mhaidat and A. Hamzah, "A New Efficient Reduction Scheme to Implement Tree Multipliers on FPGAs", in the 9th IEEE International Design and Test Symposium (IDT), Algiers, Algeria, 2014.
6. K. Mhaidat, A. Baset, and O. Al-Khaleel, "OpenSPARC Processor Evaluation using Virtex-5 FPGA and High Performance Embedded Computing (HPEC) Benchmark Suite", accepted for publication in the International Journal of Embedded and Real-Time Communication Systems (IJERTCS), October 2014.
7. K. Mhaidat, M. Alali, and I. Aljarrah, "Efficient Low-Power Compact Hardware Units for Real-Time Image and Video Processing", accepted for publication in the International Journal of Information Technology and Web Engineering (IJITWE), July 2014.
8. M. Alali, K. Mhaidat and I. Aljarrah, "Implementing image processing algorithms in FPGA hardware," in IEEE Jordan Conference on Applied Electrical Engineering and Computing Technologies (AEECT), Amman, Jordan, 2013.
9. K. Mhaidat, M. Altahat and O. Al-Khaleel, "High-Throughput Hardware Implementation of Threefish Block Cipher on FPGA," in the 4th International Conference on Information & Communication Systems (iCICS), Irbid, Jordan, 2013.
10. Inad Aljarrah, Osama Al-Khaleel, Khaldoon Mhaidat, Mu'ath Alrefai, Abdullah Alzu'bi, and Mohammad Rabab'ah, "Automated System for Arabic Optical Character Recognition with Lookup Dictionary", Journal of Emerging Technologies in Web Intelligence, Academy Publisher, Volume 4, Number 4, November 2012.
11. Inad Aljarrah, Osama Al-Khaleel, Khaldoon Mhaidat, Mu'ath Alrefai, Abdullah Alzu'bi, and Mohammad Rabab'ah, "Automated System for Arabic Optical Character Recognition", Proceedings of the 3rd International Conference on Information and Communication Systems (iCICS'12), Article No. 5, ACM, 2012.
12. Osama Al-Khaleel, Inad Aljarrah ,Abdelrahman Idries, and Khaldoon Mhaidat, "Hardware Implementation of Web Based Arabic Optical Character Recognition Units", Journal of Emerging Technologies In Web Intelligence, Volume 6, Issue 2, pp.210-219, May 2014.
13. O. Al-Khaleel, A. Idris, K. Mhaidat and I. Aljarrah, "FPGA-Based Features Extraction Unit for Arabic Characters," in The 4th International Conference on Information and Communication Systems, Irbid, Jordan, 2013.
14. Raed Bani-Hani, Salah Harb, Khaldoon Mhaidat, Eyad Taqieddin, "High-Throughput and Area-Efficient FPGA Implementations of Data Encryption Standard (DES)," Circuits and Systems Journal, SCIRP, Vol. 5, No. 3, March 2014.
15. Mohammad M. Shurman, Zaid A. Alomari, Khaldoon M. Mhaidat, "An Efficient Billing Scheme for Trusted Nodes Using Fuzzy Logic in Wireless Sensor Networks," Wireless Engineering and Technology Journal, SCIRP, Vol. 5, No. 3, July 2014.
16. O. Al-Khaleel, N. Tulic and K. Mhaidat, "FPGA implementation of binary coded decimal digit adders and multipliers," in The 8th International Symposium on Mechatronics and its Applications (ISMA), 2012.
17. Osama Al-Khaleel, Mohammad Al-Khaleel, Zakaria Al-Qudah, Christos A. Papachristou, Khaldoon Mhaidat, Francis G. Wolff, "Fast binary/decimal adder/subtractor with a novel correction-free BCD addition", 18th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2011.
18. K. Mhaidat, M. Jabri and D. Hammerstrom, "Representation, Methods, and Circuits for Time Based Conversion and Computation", International Journal of Circuit Theory and Applications, Wiley, Volume 39, Issue 3, pages 299–311, March 2011.
19. K. Mhaidat, M. Jabri and D. Hammerstrom, "Compact Low-Power Time-Based Conversion with Noise Immunity Similar to Digital Conversion", Analog Integrated Circuits and Signal Processing Journal, Springer, Volume 64, Number 2, August 2010.
20. K. Mhaidat, M. Jabri and D. Hammerstrom, "Compact Low-Power Time-Based Conversion with Noise

Immunity Similar to Digital", International Symposium on Signals Circuits and Systems (ISSCS), IEEE, July 2009.

21. Khaldoon M. Mhaidat, Marwan Jabri, Daniel Hammerstrom, “IPI Chip Design and Test Results for Synchronous IPI Based Computation and Conversion”, Semiconductor Research Corporation (SRC) report, March 2005.
22. Khaldoon M. Mhaidat, Marwan Jabri, Daniel Hammerstrom, “The Work toward an IPI Chip and VHDL-AMS Library”, SRC report, March 2004.
23. Khaldoon M. Mhaidat, Marwan Jabri, Daniel Hammerstrom, “Design of IPI Based Computation Blocks with Accuracy, Performance, and Price Analysis”, SRC report, September 2003.

UNDERGRADUATE COURSES TAUGHT

1. Microcontroller Systems (HCT, UAE)
2. Renewable Energy System (HCT, UAE)
3. Principles of Machines and Power (HCT, UAE)
4. Electrical Machines (HCT, UAE)
5. Power Generation and Distribution (HCT, UAE)
6. Power Electronics (HCT, UAE)
7. Data Communications and Networks (HCT, UAE)
8. Electrical Engineering Fundamentals (HCT, UAE)
9. Robotics Technology (HCT, UAE)
10. Electronic Circuits (HCT, UAE)
11. Electrical Circuits (HCT, UAE)
12. Circuits Lab (HCT, UAE)
13. Project Management (HCT, UAE)
14. Economics for Engineering (HCT, UAE)
15. Senior Design Project I & II (HCT, UAE)
16. Work Placement I & II (HCT, UAE)
17. Electronics-1 (PSUT)
18. Electronics-2 (PSUT)
19. Electronics Lab (PSUT)
20. Digital logic design (CPE251/CPE231)
21. Digital logic design and computer architecture for non-CPE students (CPE254)
22. Digital logic design lab (CPE253)
23. Computer organization and design (CPE252)
24. Hardware description language (HDL) lab (CPE350)
25. Microprocessor systems (CPE351/CPE353)
26. Microprocessor systems design and lab (CPE451)
27. Microprocessor interfacing lab (CPE452)
28. Computer systems project (CPE559)
29. Digital integrated circuits (CPE453/CPE420)
30. Advanced digital systems design (CPE433)
31. Computer design (CPE552)
32. Special topics in computer engineering (CPE595)
33. Graduation project I & II (JUST)
34. Practical Training I & II (JUST)
35. Microprocessor programming lab (Oregon state university)
36. Operating systems lab (Yarmouk university)
37. Microprocessor systems design (Yarmouk university)
38. Microprocessor systems design lab (Yarmouk university)

GRADUATE COURSES TAUGHT

1. System Software and Design (CPE766)
2. Parallel Computing (CPE745)
3. Real-time embedded systems (CPE746)
4. VLSI systems (CPE748)
5. Special topics in computer engineering (CPE779)
6. Computer Architecture II (NYIT EENG-741)
7. Computer systems (NYIT EENG-660)

EXAMPLES OF SENIOR DESIGN PROJECTS SUPERVISED

1. Traffic management using AI/ML
2. Health Chabot using AI/ML
3. Arabic optical character recognition (A-OCR) software
4. CMU Sphinx Arabic speech recognition (ASR) on Linux platform
5. Arabic speech recognition (ASR) on Android platform
6. Quran memorizing and learning system
7. Intrusion and malware detection software
8. Plotting Robot arm
9. Screw fastening Robot
10. Microsoft Kinect based virtual reality (VR)
11. Smart shelf with RFID
12. Autonomous/Self-Drive Vehicle
13. Imaginary keyboard

EXAMPLES OF GRADUATE COURSE PROJECTS SUPERVISED

1. Big-data Clustering using Parallel Genetic Algorithm
2. MapReduce Framework Under Virtualization Environment
3. ARM processor system prototyping and validation
4. Sun SPARC processor system prototyping and validation
5. Parallelization of RSA-CRT Algorithm using CUDA
6. RC4 stream cipher
7. AES, 3DES, IDEA, Threefish block ciphers
8. Secure Hash Algorithm SHA-256
9. Blake, Grøstl, JH, Keccak SHA-3 algorithms
10. Lightweight Hummingbird cipher
11. Mickey, Grain, Trivium stream ciphers
12. Low-power RFID system
13. ECG signal detection and classification
14. Lempel-Ziv compression
15. Karatsuba multiplication
16. Montgomery modular multiplication
17. Tree and array multipliers

EXAMPLES OF M.S. THESES SUPERVISED

1. Ahmad Baset, Title: Chip Multithreaded (CMT) Processor Validation Using Field Programmable Gate Arrays (FPGAs), 11/2010
2. Yahya Flaifel, Title: Pattern Matching Hardware Implementation using Field Programmable Gate Arrays (FPGAs), 1/2013
3. Mohammad Helail, Title: Analysis of File System Impact on Performance and Energy Consumption in Cloud Server Systems, 1/2014

4. Salah Harb, Title: FPGA based embedded system implementation of AES algorithm, 4/2014
5. Zaid Al-Omary, Title: An efficient Billing Scheme for Trusted Nodes in Wireless Sensor Networks, 5/2014
6. Mohammad Altahat, Title: Study of Performance and Power Consumption of Hypervisor Systems, 6/2014
7. Asma Bataineh, Title: Enhanced FPGA Implementations of the Scalable Montgomery Multiplication Algorithm, 6/2014
8. Abdullah Anati, Title: Performance and Power Analysis of Hypervisors in Many-Core Systems, 11/2014
9. Hiba Al-Dahoud, Title: Cryptanalysis and Improvement of Mutual Authentication Protocols in Radio Frequency Identification Systems, 12/2015
10. Heba Adnan, Title: Cryptanalysis and Enhancement of Cyclic Redundancy Check Based Mutual Authentication Protocols in RFID Systems, 8/2016
11. Ameera Al-Momany, Title: Improved Scalable Low-Latency and Low-Memory Bandwidth Radix-4 Montgomery Modular Multiplication Architecture, 5/2016
12. Mohammad Haseeba, Title: High-Level Synthesis of Convolutional Neural Network Algorithms for Image Recognition on Field Programmable Gate Arrays, In Progress.

REFERENCES

From Academia:

1. Prof. Dr. Marwan Jabri, Ph.D. supervisor at OGI/OHSU, CTO of Dillithium Networks, marwan@dilithiumnetworks.com
2. Prof. Dr. Dan Hammerstrom, Ph.D. co-supervisor at OGI/OHSU, IEEE fellow, Professor and associate dean for research, ECE, Portland State University, strom@cecs.pdx.edu
3. Prof. Alexandre Tenca, M.S. supervisor, ECE, Oregon State University, tenca@ece.orst.edu
4. Prof. Dr. Çetin Kaya Koç, M.S. co-supervisor, IEEE fellow, CS, University of California, koc@cs.ucsb.edu
5. Prof. Dr. Said Hamdioui, Chair Professor, Head of Computer Engineering Laboratory, Head of the department of Quantum and Computer Engineering, CEO and Co-Founder of CognitiveIC, Delft University of Technology, The Netherlands, S.Hamdioui@tudelft.nl, Said.Hamdioui@ieee.org
6. Prof. Dr. Baker Mohammad, Director of System-on-Chip Center and Professor of Electrical Engineering and Computer Science, Khalifa University, baker.mohammad@ku.ac.ae
7. Prof. Dr. Omar Al-Jarrah, Vice President of Arab Open University, Ex-President of JUST, Ex-President of Amman Arab University, aljarrah@just.edu.jo
8. Prof. Dr. Walid Zagalli, Division Chair of FETS, HCT, UAE, wzgallai@hct.ac.ae
9. Prof. Dr. Osama Al-Khaleel, Chairman of CPE department, JUST, oda@just.edu.jo
10. Prof. Dr. Fadi Shahroury, Chairman of EE department, PSUT, f.shahroury@psut.edu.jo

From Industry:

11. Dr. Tawfik Arabi, Manager, IEEE fellow, Intel Corporation, tawfik.r.arabi@intel.com
12. Dr. Ali Muhtaroglu, Manager, Intel Corporation, ali.muhtaroglu@intel.com
13. Dr. Christopher Pan, Manager, Intel Corporation, christopher.pan@intel.com
14. Jalal Yazdi, Manager, Intel Corporation, jalal.r.yazdi@intel.com
15. Dr. Yervant Zorian, Chief Architect and Fellow, Synopsys, IEEE fellow, yervant.zorian@synopsys.com
16. Dr. Hazem ElTahawy, Managing Director MENA Region, Mentor Graphics, hazem_eltahawy@mentor.com
17. Dr. Vazgen Melikyan, Director, Synopsys, vazgen.melikyan@synopsys.com
18. Richard Garner, IBM Global University Programs, richard@just.edu.jo
19. John McDonald, VP, Silego, jmcdonald@silego.com
20. Jeffrey Chung, Manager, Silego, jchung@silego.com