Ahmad Hiasat*

- Education
  - 1984: B. Sc. in Electrical Engineering, University of Jordan, Jordan.
  - 1988: M. Sc. in Communications Engineering, University of Jordan.
  - 1995: PhD in Systems Engineering, Oakland University, MI, USA.

- Professional Experience
  - 2012-Now: Faculty member in the Engineering School (Computer Engineering Department), Princess Sumaya University for Technology (vice President in 2013 and acting President occasionally).
  - 2011- 2012: Chairman and CEO of Electricity Regulatory Commission (ERC) of Jordan.
  - 2006- 2010: Chairman and CEO of Telecommunications Regulatory Commission (TRC) of Jordan.
  - 1996-2006: Faculty member, Princess Sumaya University for Technology (PSUT), Dean of Engineering School 2004-2006.
  - 1999-2006: part-time consultant/advisor to the Minister/Ministry of Education (MOE) on ICT in Education Reform.
  - 1993-1995: Working on PhD Program in Systems Engineering, Oakland University, Rochester, MI, USA.
  - 1985-1993: Communications Engineer and Officer, Royal Jordanian Air Force (RJAF).

- Awards and Professional Activities
  - 1984: King Hussein's Award for distinguished academic performance
  - 1988: King Hussein's Award for distinguished academic performance
  - 1995: Oakland University Award for distinguished academic performance.
  - 1996 until now: published more than 30 papers in the most prestigious international scientific journals.
  - 1996-now: reviewer for IEEE Transactions and IET Proceedings
  - 1997-now: attended and contributed to tens of ICT and Energy conferences, forums, and meetings locally and internationally.
  - 1999: Abdel Hamid Shoman Award for Young Arab Researchers in the Arab World.
  - 2000-now: contributed to formulating ICT policy, strategy and regulatory directives and instructions in ICT sector in Jordan.
  - 2001: promoted to Associate Professor

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- 2005: promoted to Full-Professor.
- 2011-now: participated in issuing and formulating main directives on Energy sector in Jordan, and specifically Energy Efficiency and Renewable Energy.
- 2015: General Chair for the IEEE AEECT 2015 conference, Nov. 3-5, 2015.
- 2015-now: Editor-in-Chief for Jordanian Journal of Computers and Information Technology (JJCIT).

• Selected Journal Publications

- A. Hiasat, "An Efficient Reverse Converter for the Three-Moduli Set $(2^{n+1}-1, 2^n, 2^n-1)$ IEEE Transactions on Circuits and Systems TCAS-II, vol. 64, no. 8, pp 962-966, August 2017. paper
- A. Hiasat, "A Residue-to-Binary Converter for the Extended Four-Moduli Set $\{2^n1, 2^n+1, 2^{2n}+1, 2^{2n+p}\}$," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 7, pp 2188-2192, July 2017. paper
- A. Hiasat, "Efficient RNS scalers for the extended three-moduli set $(2^n-1, 2^{n+p}, 2^n+1)$," IEEE Transactions on Computers, vol. 66, no. 7, pp 1253-1260, July 2017. paper
- A. Hiasat, "A Reverse Converter and Sign Detectors for an Extended RNS Five Moduli Set IEEE Transactions on Circuits and Systems TCAS-I, vol. 64, no. 1, pp 111-121, Jan. 2017. paper
- A. Hiasat, "A Sign Detector for a Group of Moduli," IEEE Transactions on Computers, vol. 65, no. 12, pp 3580 -3590 , Dec. 2016. paper
- N. Abu-Shikhah, A. Hiasat, W. Al-Rabadi, "A photovoltaic proposed generation promotion policy The case of Jordan, Energy Policy, vol. 49, no. 1, pp 154163, October 2012. paper
- A. Hiasat, "VLSI Implementation of New Arithmetic Residue to Binary De- coders," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, No. 1, pp 153-158, January 2005.
- A. Hiasat, "A Suggestion for a New RNS-based Multiplier for a Family of Moduli," International Journal of Computers and their Applications, vol. 11, no. 2, pp. 92-97, June 2004.
- A. Hiasat and A. Sweidan, "Residue to Binary Decoder for an Enhanced Moduli Set," IET Proceedings: Computers and Digital Techniques, vol. 151, no. 2, March 2004.
- O. Hasan, and A. Hiasat, "Limiter Discriminator Detection of Narrow-Band Doubinary FSK in a Land Mobile Channel," the International Journal of Communication Systems, vol. 17, no. 1, pp 85-97, February 2004.
- A. Hiasat, "A Suggestion for Fast Residue Multiplier for a Family of Moduli of the form (2n- (2p + 1))," The Computer Journal (The British Computer Society), Volume 47, Issue 1, pp. 93-102, January 2004. paper
- A. Hiasat, "Arithmetic binary to residue encoders for moduli (2n- (2p + 1))," IET Proceedings: Computers and Digital Techniques, vol. 150, no. 6, pp 369-374, November 2003.

- A. Hiasat and O. Hasan, "Bit-serial Architecture for Rank Order and Stack Filters," INTEGRATION, the VLSI Journal, Elsevier Science, Vol. 36, no. (1-2), pp 3-12, September 2003.
- A. Hiasat and A. Sweidan, "Residue Number System to Binary Converter for the Moduli Set (2n-1, 2n-1, 2n+1)," Journal of Systems Architecture, Elsevier Science, vol. 49, no. (1-2), pp. 53-58 August 2003.
- A. Hiasat, "New digital sweep oscillator structures," IET Proceedings: Cir- cuits, Devices and Systems, vol. 150, no. 3, pp 179-184, June 2003.
- A. Hiasat, "Efficient residue to binary converter," IET Proceedings: Computers and Digital Techniques, Vol. 150, No. 1, pp 11-16, January 2003.
- A. Hiasat, "High-Speed and Reduced-Area Modular Adder Structures for RNS," IEEE Transactions on Computers, Vol. 51, No. 1, pp 84-89, January 2002.
- A. Sweidan and A. Hiasat, "On the theory of error control based on moduli with common factors," Journal of Reliable Computing, Kluwer Academic, vol. 7, issue 4, p 209-218, July 2001.
- A. Hiasat, "RNS Arithmetic Multiplier for Medium and Large Moduli," IEEE Transactions on Circuits and Systems, Part II, pp 937-940, September 2000.
- A. Hiasat, "New efficient structure for a modular multiplier for RNS," IEEE Transactions on Computers, Vol. 49, No. 2, pp 170-174, February 2000.
- A. Hiasat, M. Al-Ibrahim and K. Garaibeh, "Design and implementation of a new median filtering algorithm," IET Proceedings: Vision, Image and signal Processing, vol. 146, no. 5, pp 273-278, October 1999.
- A. Hiasat and A. Al-Khateeb, "New high-resolution digital sinusoidal oscillator structure with extremely low frequency and sensitivity," Int'l J. of Electronics, vol. 86, No. 3, , pp 287-296, March 1999. paper
- A. Hiasat and H. Zohdy, "Combinational logic approach for implementing An improved approximate squaring function" IEEE Journal of Solid State Circuits, vol. 34, no. 2, pp 236-240, February 1999.
- A. Hiasat and A. Al-Khateeb, "Efficient digital sweep oscillator with extremely low sweep rates," IET Proceedings: Circuits, Devices and Systems, vol. 145,no. 6, pp 409-414, December 1998.
- A. Hiasat and H. Zohdy, "Semi-Custom VLSI design and implementation of a new efficient RNS division algorithm," The Computer Journal, vol. 42, no. 3, pp 232-240, 1999. paper
- A. Hiasat, "New designs for a sign detector and a residue to binary converter, "IET Proceedings: Circuits, Devices and Systems, pp 477-482, August 1993. paper
- A. Hiasat, "New memoryless mod (2n+1) residue multiplier," IET Electronics Letters, vol. 28, no. 3, pp 314-315, January 1992.
- A. Sweidan and A. Hiasat, "New efficient memoryless residue to binary converter, " IEEE Transactions, CAS-35, pp 1441-1444, November 1988.